

ABSTRACT OF THE DISCLOSURE

A bandgap reference generator comprises a PMOS transistor and NMOS transistor in a pnp bipolar junction transistor connected in series in a first leg. The bandgap reference generator includes a second leg that includes a PMOS transistor, an NMOS transistor, a resistor and a pnp bipolar junction transistor. A bias circuit provides a bias to a mirror formed by the gates of the PMOS transistors to lower the operating voltage of the bandgap reference generator. A second biasing circuit may provide bias to the mirror formed of the NMOS transistors. A time-based and a DC bias-based start up circuitry and method is provided.